AMENDMENT

In the Claims: **Kindly amend Claims 14, 17, 19, and 21, as follows.**

14. **(Twice Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a periphery memory region delineated on said substrate, said periphery memory region having at least one periphery memory element thereon formed;

c. a core memory region also delineated on said substrate,

said core memory region comprising at least one set of dual gate core memory structures thereon formed,

said dual gate core memory structures at least one pair of core memory stacks, and

said core memory stacks comprising:

a semiconductor material; and

a dielectric material defining respective sidewall portions;

d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said core memory stacks during etching operations, said anti-reflective coating material comprising silicon germanium (SiGe); and

e. a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect said periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.

17. **(Twice Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a periphery memory region delineated on said substrate, said periphery memory region having at least one periphery memory element thereon formed;

c. a core memory region also delineated on said substrate,

said core memory region having at least one set of dual gate core memory structures thereon formed,

said dual gate core memory structures comprising at least one pair of spaced core memory stacks, and

said core memory stacks comprising:

a semiconductor material; and

a dielectric material defining respective sidewall portions;

d. a sidewall spacer structure comprising a anti-reflective coating material for protecting said core memory stacks during etching operations, wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å); and

e. a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect said periphery memory region during etching operations and to provide a pattern for at least one periphery memory element on said periphery memory region.

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19. **(Twice Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a periphery memory region delineated on said substrate, said periphery memory region having at least one periphery memory element thereon formed;

c. a core memory region also delineated on said substrate,

said core memory region having at least one set of dual gate core memory structures thereon formed,

said dual gate core memory structures comprising at least one pair of spaced core memory stacks,

and

said core memory stacks comprising:

a semiconductor material; and

a dielectric material defining respective sidewall portions;

d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said core memory stacks during etching operations,

wherein said anti-reflective coating material comprises silicon germanium (SiGe) being compatible with ion implantation and salicidation fabrication processes, and

wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å); and

e. a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect periphery

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memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.

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21. **(Twice Amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a periphery memory region delineated on said substrate, said periphery memory region having at least one periphery memory element thereon formed;

c. a core memory region also delineated on said substrate,

said core memory region having at least one set of dual gate core memory structures thereon formed,

said dual gate core memory structures comprising at least one pair of spaced core memory stacks,

and

said core memory stacks comprising:

a semiconductor material; and

a dielectric material defining respective sidewall portions;

d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said core memory stacks during etching operations,

wherein said anti-reflective coating material comprises a material selected from a group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and silicon germanium (SiGe), said group being compatible with ion implantation and salicidation fabrication processes, and

wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., $\geq$300 Å and $<$1000 Å); and

e. a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect said periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.